CPU 206 also controls the selective enabling of PIOs 201A in step 325, thereby providing certain output signals before other output signals from CSoC 101. A more detailed description of PIOs 201A is provided in U.S. Patent Application No. 09/418,416, filed on October 15, 1999 by Triscend Corporation, and entitled "An Input/Output Circuit With User Programmable Functions."

Please replace the paragraph beginning on page 18, line 31 with the following paragraph:

Determining the states of the configuration memory cells in logic block tiles 501 is highly advantageous in debug operations. For a more detailed description of such debug operations, see U.S. Patent Application No. 09/418,948, entitled "Bus Mastering Debugging System For Integrated Circuits", filed by Triscend Corporation on October 15, 1999.

IN THE CLAIMS

The following is a clean copy of the amendments. A marked up version of the amendments is an appendix to the Amendment.

Please cancel claims 2-3 without prejudice.

Please amend the claims as follows:

1. (Amended) A method of using a system bus on a configurable system on a chip (CSoC), the CSoC including configurable system logic (CSL), the method comprising:

determining if the system bus is controlled for configuration by a first device selected from a group consisting of on-chip central processing unit (CPU), direct memory access (DMA) controller, and external control device;

configuring a memory cell in the CSL using the system bus; and

reading the memory cell in the CSL using the system bus.

Please add the following new claims:

14. (New) The method of claim 1 further comprising:

mapping the memory cell in the CSL into an addressable memory space of the system bus.

15. (New) The method of claim 14 wherein reading a memory cell in the CSL using the system bus is performed by a second device selected from the group consisting of on-chip central processing unit (CPU), direct memory access (DMA) controller, and external control device.

16. (New) The method of claim 15 further comprising:

mapping a random access memory (RAM) cell in the CSoC in to the addressable memory space of the system bus.

17. (New) The method of claim 16 further comprising:

reading the RAM cell using the system bus.

18. (New) The method of claim 17 wherein reading the RAM cell using the system bus is performed by a third device selected from the group consisting of on-chip central processing unit (CPU), direct memory access (DMA) controller, and external control device.

19. (New) The method of claim 1 wherein the system bus is used for configuration and general interconnect.

20. (New) The method of claim 19 further comprising:

selecting a signal with a multiplexer in the CSoC to determine if the system bus is used for configuration or general interconnect.

Please add the following new claims:

14. (New) The method of claim 1 further comprising:

mapping the memory cell in the CSL into an addressable memory space of the system bus.

15. (New) The method of claim 14 wherein reading a memory cell in the CSL using the system bus is performed by a second device selected from the group consisting of on-chip central processing unit (CPU), direct memory access (DMA) controller, and external control device.

16. (New) The method of claim 15 further comprising:

mapping a random access memory (RAM) cell in the CSoC in to the addressable memory space of the system bus.

17. (New) The method of claim 16 further comprising:

reading the RAM cell using the system bus.

18. (New) The method of claim 17 wherein reading the RAM cell using the system bus is performed by a third device selected from the group consisting of on-chip central processing unit (CPU), direct memory access (DMA) controller, and external control device.

19. (New) The method of claim 1 wherein the system bus is used for configuration and general interconnect.

20. (New) The method of claim 19 further comprising:

selecting a signal with a multiplexer in the CSoC to determine if the system bus is used for configuration or general interconnect.